IN THE SPECIFICATION:

Page 8, line 5

According to a preferred embodiment of the present invention, CPU 110 executes a new instruction by fetching an instruction stored in main program memory (MPM) 140. An address, preferably 16 bits, is sent via address bus 130 to main program memory 140 and coprocessor program memory (CPM) 160. Main program memory 140 and CPM 160 output the addressed instruction onto processor data bus 150, and the instruction read from MPM 140 is buffered at CPU fetch buffer 111 and then is latched into Instruction Register (IR) 114 of CPU 110. The coprocessor instruction read from CPM 160 is 'n' bits, preferably 16 bits, which represent the ~~LSB~~ least significant bits (LSBs) portion of the entire coprocessor instruction. The n-bit instruction is buffered by coprocessor fetch buffer 126 and then latched by coprocessor instruction register 121 of coprocessor 120. The latching of the coprocessor instruction in register 121 will be synchronized to the system clock. This process will be further described below. It is known to one skilled in the art that coprocessor type instructions can be signalled in the 'c' most significant bits (MSBs) of the instruction. For purposes of illustration, the first 3 bits, or c=3, is used in the present embodiment. It is also readily apparent that the 16-bit address format, serves to illustrate the exemplary embodiment, but the device and method of the present invention is applicable to any number of addressing bits, any distribution of addressing between the main processor or coprocessing addressing, any number of bit width for the CPU or coprocessor instruction, and any designation of which of the address bits are used to signal a coprocessor operation.